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EXAMINER	
BANANKHAH, MAJID A	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/606,839	KARDACH, JAMES P.	
	Examiner	Art Unit	
	Majid A. Banankhah	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This non-office action is in response to amendment, filed April 23, 2004. Application's argument has been fully considered but they are moot in view of the new ground of rejection.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11, 13-15, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald (U.S. Pat. No. 6,295,574, hereinafter MacDonald) in view of Simpson (EP0742522A, hereinafter Simpson), and further in view of Maupin (U.S. Pat. No. 6,154,832, hereafter maupin).

Per claim 1, teaches, Receiving a real time analog data (col. 5, lines 17-32, RT peripheral 114, data measured from a device) at a personal computer (Fig. 1, CPU 102) implementing a general purpose operating system (multi-tasking operating system, col. 1, lines 15-26),

generating real time interrupt indicating a request to process real-time data at a central processing unit (col. 5, lines 33-54, interrupt service routine RTI peripheral 114, and

processing time within the device cannot exceed the sample interval [real-time], CPU 102, see also, col. 3, lines 46-63); and

While the system of MacDonald suggesting the highest priority assignment to be given to real time interrupts but fails to teach of a step or means for determining the real time interrupts among the interrupts (real time and non real time). However, the reference of Simpson teaches of a method and means for handling multiple priority interrupt requests wherein arbitration circuit is provided for determining a priority status for each interrupt signal with the highest priority status and output circuitry, and an outputting circuitry, operable to output an interrupt signal only in response to an interrupt signal having a higher priority status than any currently executing interrupt process (see, Simpson (see, col. 1, lines 34-56).
processing the real-time event if the real time interrupt has a higher priority than the non real time operation (col. 1, lines 34-56). Non real time operation is any operation such as currently executing interrupt process in the above-cited paragraph.

Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use priority determination scheme of Simpson in the real time interrupt handling system of MacDonald, for the reason to be able to direct processors attention to high priority real time data than processing the less urgent or non real time data. Simpson suggests the motivation in col. 1, lines 22-29.

Additionally, the reference of McDonald in view of Simpson, does not clearly indicate that higher priority is assigned to real-time to real-time interrupts. However, Maupin explicitly teach of a system in which the processor includes an execution core configured to execute instructions and register file coupled to the execution core. The register file is divided into a plurality of register sets, and one of the plurality of register sets is dedicated to a default task, and each remaining one of plurality of register sets is

dedicated to different interrupt source (col. 2, lns. 56-64). Later Maupin teach that high priority be assigned to real-time interrupts (col. 7, lns. 21-35, the defined order may correspond to a priority scheme amongst the possible interrupt sources. For example, those interrupt sources which are "real-time" in nature (i.e. the interrupt source operates according to real-time as opposed to devices which may operate properly with any latency) may be defined as high priority while non-real-time interrupt sources may be lower priority. For example, video and audio devices are typically real-time devices.), for the reason not to delay real-time devices and cause a real time task wait while a non real time task is running. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to assign high priority to real time interrupts as opposed to non-real time interrupts.

As to claim 2, continuing processing the first event if the real-time event does not have a higher priority than the first process. In the system of Simpson, by default, when there is no higher priority interrupt than the currently running process (operation), the priority of the running process is higher and therefore, the process continue to run without interruption (Simpson, Abstract, interrupt identifier is operable only in response to interrupt signals having a higher priority status than any currently executing interrupt process). Therefore, even though the interrupt is present, since the priority of the interrupt is not higher than the priority of the currently running process, the currently running task is not interrupted because the identifier circuit does not identify that.

Per claim 3, the context and state of the executing task is saved before the

interrupt service routine is executed and the states are restored after execution of the real time [high priority] data is executed (see, MacDonald, col. 43-63, and col. 2, lines 18-39).

Per claims 4 and 5 are rejected for the reason explained in the rejection of claim 1. The method of Simpson, determine the priority among interrupts and make a determination as to which interrupt has the highest priority (see, Simpson, col. 1, lines 34-56). It is obvious that the processing will continue if the priority of the real time is not higher than the priority of the real time, because the arbiter looks at the priority and does not know whether the data is real time or not.

Per claim 6, the claim is rejected for the reasons stated in the rejection of claim 4, and the reference of Simpson further teaches of returning to execution of the interrupted process, meaning that the interrupted process is terminated when the arbiter receives a higher priority interrupt.

Per claim 7, a chipset (Fig. 1, 100), a bus coupled to the chipset (bus bridge 106); and a central processing unit (CPU), coupled to the bus (CPU 102), to generate a real time interrupt upon receiving real time analog data (col. 5, lines 33-54, interrupt service routine RTI peripheral 114, and processing time within the device cannot exceed the sample interval [real-time], CPU 102).

While the system of MacDonald suggesting the highest priority assignment to be given to real time interrupts but fails to explicitly teach of processing data associated with real time interrupt if the real time interrupt has a higher priority than a non real time operation currently being processed. However, the reference of Simpson teaches of a method and means for handling multiple priority interrupt requests wherein arbitration circuit is provided for determining a priority status for each interrupt signal with the

highest priority status and output circuitry, and an outputting circuitry, operable to output an interrupt signal only in response to an interrupt signal having a higher priority status than any currently executing interrupt process (see, Simpson (see, col. 1, lines 34-56). processing the real-time event if the real time interrupt has a higher priority than the non real time operation (col. 1, lines 34-56). Non real time operation is any operation such as currently executing interrupt process in the above-cited paragraph.

Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use priority determination scheme of Simpson in the real time interrupt handling system of MacDonald, for the reason to be able to direct processors attention to high priority real time data than processing the less urgent or non real time data. Simpson suggests the motivation in col. 1, lines 22-29.

Per claim 8, timer is inherent in an interrupt service routine disclosed in MacDonald (See also col. 3, lines 35-44, clock cycle), and generating real time interrupt is taught in col. 3, lines 46-63.

Per claim 9, processing real time interrupt is taught by MacDonald in col. 3, lines 46-63 (RTI), Simpson teaches of detail of an interrupt handler (see, Simpson col. 8, lines 9-42).

Per claim 10, register to store real time data is shown by MacDonald (see Abstract, registers allocated for real time use are indicated in the RTI register).

Per claim 11, as discussed in the rejection of claim 1, the reference of Simpson teaches of relative priority between real time interrupt and non real time operation.

Per claim 13, the claim is rejected for the reasons stated in the rejection of claims 8-10.

Per claims 14 and 20 using radio signal, as analog data does not modify the method of MacDonald, therefore, it is obvious to use radio signal as analog data if this is users desire.

Per claim 15, Simpson teaches of interrupt handler in col. 1, lines 34-65 (indication is held by storage circuitry and selecting the one interrupt signal with highest priority status).

Per claim 19 and generating real time interrupt in response to receiving timing signal from the timer is taught by MacDonald in col. 3, lines 46-63.

5. Claims 12, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald (U.S. Pat. No. 6,295,574, hereinafter MacDonald) in view of Simpson (EP0742522A, hereinafter Simpson), further in view of Williams et al. (U.S. Pat. No. 5,764,582).

Per claims 12 and 16 the modified MacDonald fails to explicitly teach of analog to digital converter, However, the use of analog to digital converter is well known in the art as it is evidenced by Williams, in col. 4, lines 1-37 (D/A and A/D converters), for the reason to be able to process analog data and convert analog into digital. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use Williams's analog to digital converter.

Per claim 17, registering is taught by MacDonald in the abstract, and col. 3, line 64 to col. 4, line 5.

Per claim 18, the timing signal is created by the clock cycle, and MacDonald teaches storing the interrupting the register in col. 3, lines 46-63.

6. Applicant on pages 7 of the Remarks arguing, "Claims I-11. 13-15. and 19-20 were improperly rejected because MacDonald in view of Simpson does not disclose determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at a CPU". Later on page 8, arguing that "In fact, the Examiner, in the Final Office Action admits that MacDonald fails to explicitly teach of a step or means for determining the real time interrupt has a higher priority than a non-real time operation being processed at the CPU. See Final Office Action, mailed November 18, 2004, at page 3, paragraph 1. Instead, the Examiner cites Simpson as including such a feature.

In response, McDonald teaches of a real-time interrupt control unit to control real time interrupt capabilities of the CPU. He also suggest that real-time interrupt be given highest priority (col. 6, In. 68 to col. 7, 1n.2, preferably, the real-time interrupt is the highest priority interrupt within CPU). This is also indicated and suggested by the new reference of Maupin, i.e., real-time is given the highest priority (col. 7, Ins. 21-35), used in the rejection of claim to show that it is common practice by artisans to assign the real time interrupts the highest priority. Now keeping that in mind, Simpson has a system that can select between a higher priority interrupt amongst low and high priorities. Since, according to McDonald, and Maupin, highest priority is given to real-time interrupts, the system of Simpson simply can determine the highest priority interrupts (which are the real-time interrupts) amongst the real time and non real time priorities. The system of Simpson does not know and care less if the highest priority is real time or not real time.

Simpson selects higher priority amongst some interrupt signals. Now if the real-time interrupts have higher priority (as claimed by applicant), Simpson obviously can and will select that simply because, it does have the highest priority. Hence, Simpson can determine whether a the real-time interrupt has a higher priority than a non real-time operation being processed at the CPU, since the highest priority is suggested to be given to real time interrupts, by McDonald and Maupin.

On page 9, applicant arguing that "Simpson further discloses arbiter circuitry connected to storage circuitry for determining the priority status for each interrupt signal. See Simpson at col. 1, 11. 46-48. Nonetheless, Simpson does not disclose or suggest determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at a CPU".

In response, as stated above, and admitted by applicant, Simpson can determine whether an interrupt has a higher priority than another interrupt. Since, by McDonald, and Maupin's suggestion, real-time interrupts are ordinarily given the highest priority, obviously can determine whether a real-time interrupts has a higher priority than a non real-time priority. The system of Simpson does not know, and does not need to know whether the higher priority is give to real-time interrupts or non real-time interrupts. All he needs to know is which interrupts has a higher priority. Now if the highest priorities are assigned to real-time interrupts, obviously Simpson can determine which one (the real time interrupts) has a higher priority.

Later on the same page applicant arguing that "Even though Simpson discloses a processor interrupt control system that determines the priority of interrupts, the interrupts are not real-time interrupts. Real-time interrupts are very time sensitive and therefore require much faster processing than do non real-time interrupts. A system designed to handle non real-time interrupts, as disclosed in Simpson, could not be used to handle the addition of real-time interrupts".

In response, applicant must show that in a system where the higher priority is given to real-time interrupt, whey Simpson cannot determine a real-time interrupt has a higher priority than a non real-time interrupt. The system of Simpson can do priority determination amongst "non real-time interrupts" as well as "real-time and non real-time interrupts".

On page 11, applicant arguing that "Nevertheless, Williams does not disclose or suggest determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at a CPU. Since MacDonald and Simpson fail to disclose all of the elements included in the appellant's independent claim including claim 1, claim 1, and since Williams fails to disclose or suggest those elements missing from MacDonald and Simpson, the combination of MacDonald, Simpson, and Williams fails to disclose or suggest each and every element of the Appellant's invention as embodied in the claims. Consequently, the Examiner has not established a prima facie case of obviousness, and the Examiner's rejection of claims 12 and 16-18 under 35 U.S.C. 103(a)

as being obvious over the combination of MacDonald, Simpson, and Williams should be reversed".

In response, since Williams is cited in this rejection in combination with MacDonald and Simpson, it must be pointed out that this reference is used primarily to show that analog to digital and digital to analog converters are well known in the art. One cannot show non-obviousness by attacking the references separately. The Examiner is not relying on this reference to show real-time interrupt handling features. This reference is used to show that analog to digital conversion is well known in the art.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Majid A. Banankhah** whose telephone number is (571) **272-3770**. The examiner can normally be reached on Monday – Friday, 7:00 AM – 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Meng-Ai An** can be reached on (571) 272-3756.

Any inquiry of a general nature or relating to the status of this application should be directed to the **TC2100 Group** receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Maid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:
Commissioner of Patent and Trademarks

Washington, D.C. 20231

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Maid Banankhah

6/25/04

MAJID BANANKHAH
PRIMARY EXAMINER